REMARKS

This is a full and timely response to the outstanding final Office Action mailed on May 19, 2008 (Paper No. 20080511). Upon entry of this response, claims 1, 3-6, and 8-19 are pending in the application. In this response, claims 1, 4, and 19 have been amended. Applicants respectfully request that the amendments being filed herewith be entered and request reconsideration and allowance of all pending claims.

I. Improper FINAL Office Action

The Office Action states on page 12 that "THIS ACTION IS MADE FINAL." Applicants respectfully submit that the Office Action mailed on May 19, 2008, is not a proper final Office Action under MPEP § 706.07. MPEP § 706.07 states:

> Before final rejection is in order a clear issue should be developed between the examiner and applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public, the invention as disclosed and claimed should be thoroughly searched in the first action and the references fully applied...

Specifically, the MPEP points out in § 707.07(d) that "Where a claim is refused for any reason relating to the merits thereof it should be "rejected" and the ground of rejection fully and clearly stated...".

The Office Action mailed on November 27, 2007, on page 3, rejected claims 1, 3-6, and 8-19 as allegedly anticipated by the *Malik et al.* reference. In explanation, the Office Action copied the Applicants' claim language and indicated that all elements were taught in the *Malik et al.* reference, i.e. "see abstract and paragraphs 13-16, 19 and figures 1, 2 and 5", without further clarification. As such, the Office Action did not fully and clearly state the grounds for rejection of the claims. A broad-brush statement that each of the multiple limitations are taught somewhere in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" of the *Malik et al.* reference denied the Applicant a full opportunity to address and refute rejection of Applicants' claims. In

other words, without a specific identification of how the *Malik et al.* reference anticipated each of the specific limitations, it is not possible to fully respond to an Office Action rejection given that the true basis for the rejection is not ascertainable.

The lack of clarity was addressed on pages 8-11 of the Response to the Office Action mailed on November 27, 2007, which Applicants filed on February 15, 2008. As a result, the Examiner provided additional details regarding the rejection of claim 1 in the Response to Arguments section of the Office Action mailed on May 19, 2008. Only after receiving the additional details did Applicants fully appreciate the Examiner's application, of the cited art, and this more complete understanding has led Applicant to submit the amendments made herein. Therefore, in fairness, Applicant submits that these amendments should be entered. Indeed, Applicant submits that the status of FINAL should be withdrawn from the previous Office Action, so that the amendments can be entered, and any FINALity not be levied on this application until after the Examiner's consideration of this submission.

II. Claim Rejections under 35 U.S.C. §102(e)

Claims 1, 3-6, and 8-19 have been rejected under 35 U.S.C. § 102(e) as allegedly anticipated by *Malik et al.* (U.S. Patent Application Pub. No. 2004/0260908, hereafter "*Malik*"). Applicants respectfully traverse this rejection as applied to pending claims 1, 3-6, and 8-19.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP § 2131 *quoting Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(e). In the present case, not every feature of the amended claims is represented in the *Malik* reference.

A. Independent Claim 1

Applicants' amended claim 1 provides as follows (emphasis added):

> A method comprising:
> determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the first I/O device and a memory device;
> ***providing buffer allocation information to the first I/O device responsive to the at least one characteristic of the first I/O device***;
> buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion corresponding to the buffer allocation information provided to the first I/O device;
> determining at least one characteristic of a second I/O device that is coupled to the memory device interface;
> ***providing buffer allocation information to the second I/O device responsive to the at least one characteristic of the second I/O device***; and
> buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion corresponding to the buffer allocation information provided to the second I/O device.

Applicants respectfully submit that amended independent claim 1 is allowable for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in amended claim 1.

While *Malik* discloses:

> In operation, any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... The read request from the master is seen by the memory controller 20. The read request has one or more attributes such as the Data Size and Burst Length. The memory controller is aware of the master ID, the data size being requested and a requested burst length as well as a memory address. The Burst Length signal communicates to the memory controller 20 whether the requested operation is a burst operation. Based on the information in the memory controller interconnect, if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...
>
> If the address does not hit in the prefetch buffer 30 and misses, based on whether the requesting master is enabled for prefetching, dynamic configuration of the prefetch buffer line size occurs based on data size and burst length. An adaptive buffer line replacement algorithm... selects which buffer line is replaced and new data written to. The prefetch control

> circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

(*Malik* at paragraphs 14-15), *Malik* does not teach or suggest "providing buffer allocation information to the ... I/O device" as recited in amended claim 1. Thus, *Malik* does not disclose, teach or suggest either "providing buffer allocation information to the first I/O device responsive to the at least one characteristic of the first I/O device" or "providing buffer allocation information to the second I/O device responsive to the at least one characteristic of the second I/O device" as recited in amended claim 1.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in amended claim 1. Therefore, Applicants respectfully submit that the rejection of claim 1 be withdrawn.

B. Dependent Claims 3-5

Since independent claim 1 is allowable, Applicants respectfully submit that claims 3-5 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir.1988). Therefore, Applicants respectfully request that the rejection of claims 3-5 be withdrawn.

C. Dependent Claim 3

Applicants' claim 3 provides as follows (emphasis added):

> The method of claim 1, further comprising:
> ***receiving data from the first I/O device via a first data transfer link***; and
> ***receiving data from the second I/O device via a second data transfer link***.

Notwithstanding, and in addition to, the arguments discussed above, Applicants respectfully request that the rejection of claim 3 be withdrawn for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 3.

The Office Action alleges that *Malik* teaches all of the features of claim 3 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 6). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, and a second I/O device corresponds to element 14 (master 2) of FIG. 1 (Office Action at pages 2-3).

In particular, *Malik* teaches that:

> any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...
>
> If the address does not hit in the prefetch buffer 30 and misses... prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

(*Malik* at paragraphs 14-15). While *Malik* teaches providing data to the requesting master, *Malik* does not teach or suggest "receiving data from the ... I/O device" as recited in claim 3. Thus, *Malik* does not disclose, teach or suggest either "receiving data from the first I/O device via a first data transfer link" or "receiving data from the second I/O device via a second data transfer link" as recited in claim 3.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 3. Therefore, Applicants respectfully submit that the rejection of claim 3 be withdrawn.

D. Dependent Claim 4

Applicants' claim 4 provides as follows (emphasis added):

> The method of claim 1, further comprising:
> ***receiving a first data unit from the first I/O device***;
> ***buffering the first data unit in the first portion of the buffer***;
> ***transferring the first data unit to the memory device***;
> ***receiving a second data unit from the second I/O device***;

buffering the second data unit in the second portion of the buffer; and
transferring the second data unit to the memory device.

Notwithstanding, and in addition to, the arguments discussed above, Applicants respectfully request that the rejection of claim 4 be withdrawn for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 4.

The Office Action alleges that *Malik* teaches all of the features of claim 4 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 6). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, a memory device corresponds to elements 22, 24, and 26 (memory 1-3), a first portion of a buffer of the memory device interface corresponds to element 36 (burst line) of FIG. 2, a second I/O device corresponds to element 14 (master 2) of FIG. 1, and a second portion of the buffer corresponds to element 40 (burst line) of FIG. 2 (Office Action at pages 2-4).

For the reasons discussed in section I.C above, while *Malik* teaches providing data to the requesting master, *Malik* does not teach or suggest either "receiving a first data unit from the first I/O device" or "receiving a second data unit from the second I/O device" as recited in claim 4. In addition, while *Malik* teaches that "data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26" (*Malik* at paragraph 16), *Malik* does not disclose or suggest buffering a data unit received from an I/O device in a portion of the buffer. Nor does *Malik* disclose or suggest transferring data to memories 22, 24, and 26. Thus, *Malik* does not teach or suggest either "buffering the first data unit in the first portion of the buffer; transferring the first data unit to the memory device; [or] ... buffering the second data unit in the second portion of the buffer; and transferring the second data unit to the memory device" as recited in claim 4.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 4. Therefore, Applicants respectfully submit that the rejection of claim 4 be withdrawn.

E. Independent Claim 6

Applicants' claim 6 provides as follows (emphasis added):

> A method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising:
> ***buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface***;
> ***buffering data received via a second data transfer link in a second portion of the buffer***, a buffering capacity of the first portion being different than a buffering capacity of the second portion; and
> wherein the buffering capacity of the first portion is responsive to at least one characteristic of ***a first I/O device that provides data to the memory device interface via the first data transfer link***, and the buffering capacity of the second portion is responsive to at least one characteristic of ***a second I/O device that provides data to the memory device interface via the second data transfer link***.

Applicants respectfully submit that independent claim 6 is allowable for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 6.

The Office Action alleges that *Malik* teaches all of the features of claim 6 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at pages 7-8). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, a memory device corresponds to elements 22, 24, and 26 (memory 1-3), a first portion of a buffer of the memory device interface corresponds to element 36 (burst line) of FIG. 2, a second I/O device corresponds to element 14 (master 2) of FIG. 1, and a second portion of the buffer corresponds to element 40 (burst line) of FIG. 2 (Office Action at pages 2-4).

In particular, *Malik* teaches that:

> any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...
>
> If the address does not hit in the prefetch buffer 30 and misses... prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

(*Malik* at paragraphs 14-15). While *Malik* teaches providing data to the requesting master, *Malik* does not teach or suggest an "I/O device that provides data to the memory device interface" as recited in claim 6. Thus, *Malik* does not disclose, teach or suggest either "a first I/O device that provides data to the memory device interface via the first data transfer link" or "a second I/O device that provides data to the memory device interface via the second data transfer link" as recited in claim 6.

Furthermore, while *Malik* teaches that "data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26" (*Malik* at paragraph 16), *Malik* does not disclose or suggest buffering data received from an I/O device in a portion of the buffer. Thus, *Malik* does not teach or suggest either "buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface" or "buffering data received via a second data transfer link in a second portion of the buffer" as recited in claim 6.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 6. Therefore, Applicants respectfully submit that the rejection of claim 6 be withdrawn.

F. Dependent Claims 8-9

Since independent claim 6 is allowable, Applicants respectfully submit that claims 8-9 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*,

837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir.1988). Therefore, Applicants respectfully request that the rejection of claims 8-9 be withdrawn.

G. Dependent Claim 8

Applicants' claim 8 provides as follows (emphasis added):

> The method of claim 6, further comprising:
> ***receiving a first data unit from the first I/O device via the first data transfer link***;
> ***buffering the first data unit in the first portion of the buffer***;
> ***transferring the first data unit to the memory device***;
> ***receiving a second data unit from the second I/O device via the second data transfer link***;
> ***buffering the second data unit in the second portion of the buffer***; and
> ***transferring the second data unit to the memory device***.

Notwithstanding, and in addition to, the arguments discussed above, Applicants respectfully request that the rejection of claim 8 be withdrawn for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 8.

The Office Action alleges that *Malik* teaches all of the features of claim 8 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 8). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, a memory device corresponds to elements 22, 24, and 26 (memory 1-3), a first portion of a buffer of the memory device interface corresponds to element 36 (burst line) of FIG. 2, a second I/O device corresponds to element 14 (master 2) of FIG. 1, and a second portion of the buffer corresponds to element 40 (burst line) of FIG. 2 (Office Action at pages 2-4).

For the reasons discussed in section I.E above, while *Malik* teaches providing data to the requesting master, *Malik* does not teach or suggest either "receiving a first data unit from the first I/O device" or "receiving a second data unit from the second I/O device" as recited in claim 8. In addition, while *Malik* teaches that "data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26" (*Malik* at paragraph 16), *Malik* does not

disclose or suggest buffering a data unit received from an I/O device in a portion of the buffer. Nor does *Malik* disclose or suggest transferring data to memories 22, 24, and 26. Thus, *Malik* does not teach or suggest either "buffering the first data unit in the first portion of the buffer; transferring the first data unit to the memory device; [or] ... buffering the second data unit in the second portion of the buffer; and transferring the second data unit to the memory device" as recited in claim 8.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 8. Therefore, Applicants respectfully submit that the rejection of claim 8 be withdrawn.

H. Independent Claim 10

Applicants' claim 10 provides as follows (emphasis added):

> A memory device interface that is configured to enable data transfers between an input/output (I/O) device, ***the memory device interface comprising***:
> a buffer;
> ***a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device***; and
> ***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device***, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

Applicants respectfully submit that independent claim 10 is allowable for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 10.

The Office Action alleges that *Malik* teaches all of the features of claim 10 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 9). In particular, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, a first portion of a buffer of the memory device interface corresponds to element 36 (burst line) of

FIG. 2, a second I/O device corresponds to element 14 (master 2) of FIG. 1, and a second portion of the buffer corresponds to element 40 (burst line) of FIG. 2 (Office Action at pages 2-4).

Specifically, *Malik* teaches that "Memory controller 20 contains a prefetch buffer 30 and prefetch control circuitry 32" (*Malik* at paragraph 13 and FIG. 1).

> Illustrated in FIG. 2 is a diagram of a portion of a configuration of the prefetch buffer 30 based upon different burst length support. In the illustrated form, a plurality of burst blocks or burst lines, such as burst lines 36, 38, 40, 42, 44 and 46, is provided. ... Within each burst line, such as burst line 36 is a status field and a predetermined number of data words in a data field 50. ... It should be understood that the data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26 than the data from burst line 36. The same is true with respect to the source of data in all of the other illustrated burst lines. The particular configuration of prefetch buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and the Burst Length signal. The Data Size signal determines the size of a single unit of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. ... in the illustrated portion of prefetch buffer 30 of FIG. 2, the buffer storage area is dynamically configurable, based on the requested accesses to be serviced. ... the buffers may be dynamically configured into any combination of lengths as access requests are received. Dynamic configuration of the buffers may be based at least in part on the Data Size and Burst Length signals.
>
> Illustrated in FIG. 5 is a further detail of one implementation 70 of the prefetch control circuitry 32 of FIG. 1. Dynamic Buffer Configuration logic 72 has a first input for receiving the Data Size attribute signal, a second input for receiving the Burst Length attribute signal, a third input for receiving the Bus Width signal from an addressed memory, such as memory 22, 24 or 26. A first output of the Dynamic Buffer Configuration logic 72 is connected to an input of Adaptive Buffer Store Replacement logic 74. An output of the Adaptive Buffer Store Replacement logic 74 provides a buffer portion replacement indicator and is connected to a first input of Request Type logic 76. A second output of the Dynamic Buffer Configuration logic 72 is connected to a second input of the Request Type logic 76. An output of the Request Type logic 76 is connected to one of the three Memory Interconnects of FIG. 2.

(*Malik* at paragraphs 16 and 19). *Malik* does not mention registers, much less "registers ... configured to enable the memory device interface to buffer in a ... portion of the buffer data" as alleged. Thus, *Malik* does not disclose or suggest "the memory device interface comprising... a

first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device; and a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device" as recited in claim 10.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 10. Therefore, Applicants respectfully submit that the rejection of claim 10 be withdrawn.

I. Dependent Claims 11-14

Since independent claim 10 is allowable, Applicants respectfully submit that claims 11-14 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir.1988). Therefore, Applicants respectfully request that the rejection of claims 11-14 be withdrawn.

J. Dependent Claim 12

Applicants' claim 12 provides as follows (emphasis added):

> The memory device interface of claim 10, wherein the first plurality of registers comprises:
> ***a first buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer***; and
> ***a second buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the second I/O device to be buffered in the second portion of the buffer***.

Notwithstanding, and in addition to, the arguments discussed above, Applicants respectfully request that the rejection of claim 12 be withdrawn for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 12.

The Office Action alleges that *Malik* teaches all of the features of claim 12 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at pages 9-10). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG.

1, a memory device corresponds to elements 22, 24, and 26 (memory 1-3), a first portion of a buffer of the memory device interface corresponds to element 36 (burst line) of FIG. 2, a second I/O device corresponds to element 14 (master 2) of FIG. 1, and a second portion of the buffer corresponds to element 40 (burst line) of FIG. 2 (Office Action at pages 2-4).

In particular, *Malik* teaches that:

> any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...
>
> If the address does not hit in the prefetch buffer 30 and misses... prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

(*Malik* at paragraphs 14-15). While *Malik* teaches providing data to the requesting master, *Malik* does not teach or suggest "data received from the ... I/O device to be buffered in the ... portion of the buffer" as recited in claim 12. Thus, *Malik* does not disclose, teach or suggest "a buffer allocation value that is configured to enable data received from the ... I/O device to be buffered in the ... portion of the buffer" as recited in claim 12. In addition, even though *Malik* discloses "An output of the Adaptive Buffer Store Replacement logic 74 provides a buffer portion replacement indicator", *Malik* does not teach or suggest that the replacement indicator "is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer". Therefore, *Malik* does not disclose or suggest either "a first buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the first I/O device to be buffered in the first portion of the buffer" or "a second buffer allocation counter that specifies a buffer allocation value that is configured to enable data received from the second I/O device to be buffered in the second portion of the buffer" as recited in claim 12.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 12. Therefore, Applicants respectfully submit that the rejection of claim 12 be withdrawn. Additionally, Applicants respectfully submit that claims 13-14 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir.1988).

K. Dependent Claim 13

Applicants' claim 13 provides as follows (emphasis added):

> The memory device interface of claim 12, wherein ***the value of the first buffer allocation counter is decremented responsive to a buffer allocation value being sent to the first I/O device***.

Notwithstanding, and in addition to, the arguments discussed above, Applicants respectfully request that the rejection of claim 13 be withdrawn for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 13.

The Office Action alleges that *Malik* teaches all of the features of claim 13 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 10). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1 and a memory device interface corresponds to element 20 (memory controller) of FIG. 1 (Office Action at page 2).

While *Malik* discloses:

> In operation, any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... The read request from the master is seen by the memory controller 20. The read request has one or more attributes such as the Data Size and Burst Length. The memory controller is aware of the master ID, the data size being requested and a requested burst length as well as a memory address. The Burst Length signal communicates to the memory controller 20 whether the requested operation is a burst operation. Based on the information in the memory controller interconnect, if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...

> If the address does not hit in the prefetch buffer 30 and misses, based on whether the requesting master is enabled for prefetching, dynamic configuration of the prefetch buffer line size occurs based on data size and burst length. An adaptive buffer line replacement algorithm... selects which buffer line is replaced and new data written to. The prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

(*Malik* at paragraphs 14-15), *Malik* does not teach or suggest "a buffer allocation value being sent to the first I/O device" as recited in amended claim 13. In addition, even though *Malik* discloses "An output of the Adaptive Buffer Store Replacement logic 74 provides a buffer portion replacement indicator", *Malik* does not teach or suggest that the replacement indicator "is decremented", much less "decremented responsive to a buffer allocation value being sent to the first I/O device" as recited in claim 13. Thus, *Malik* does not disclose, teach or suggest "the value of the first buffer allocation counter is decremented responsive to a buffer allocation value being sent to the first I/O device" as recited in claim 13.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 13. Therefore, Applicants respectfully submit that the rejection of claim 13 be withdrawn. Additionally, Applicants respectfully submit that claim 14 is allowable for at least the reason that it depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir.1988).

L. Independent Claim 15

Applicants' claim 15 provides as follows (emphasis added):

> ***A memory device interface comprising***:
> a buffer;
> ***a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link***; and
> ***a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link***, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

Applicants respectfully submit that independent claim 15 is allowable for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 15.

The Office Action alleges that *Malik* teaches all of the features of claim 15 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 10). In particular, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, a first portion of a buffer of the memory device interface corresponds to element 36 (burst line) of FIG. 2, a second I/O device corresponds to element 14 (master 2) of FIG. 1, and a second portion of the buffer corresponds to element 40 (burst line) of FIG. 2 (Office Action at pages 2-4).

Specifically, *Malik* teaches that "Memory controller 20 contains a prefetch buffer 30 and prefetch control circuitry 32" (*Malik* at paragraph 13 and FIG. 1).

> Illustrated in FIG. 2 is a diagram of a portion of a configuration of the prefetch buffer 30 based upon different burst length support. In the illustrated form, a plurality of burst blocks or burst lines, such as burst lines 36, 38, 40, 42, 44 and 46, is provided. ... Within each burst line, such as burst line 36 is a status field and a predetermined number of data words in a data field 50. ... It should be understood that the data from burst line 36 may have been retrieved from a same or a different one of the memories 22, 24 and 26 than the data from burst line 36. The same is true with respect to the source of data in all of the other illustrated burst lines. The particular configuration of prefetch buffer 30 is created by the prefetch control circuitry 32 in response to the Data Size signal and the Burst Length signal. The Data Size signal determines the size of a single unit of data within each burst line. The Burst Length signal determines the number of single units of data per burst line. ... in the illustrated portion of prefetch buffer 30 of FIG. 2, the buffer storage area is dynamically configurable, based on the requested accesses to be serviced. ... the buffers may be dynamically configured into any combination of lengths as access requests are received. Dynamic configuration of the buffers may be based at least in part on the Data Size and Burst Length signals.
>
> Illustrated in FIG. 5 is a further detail of one implementation 70 of the prefetch control circuitry 32 of FIG. 1. Dynamic Buffer Configuration logic 72 has a first input for receiving the Data Size attribute signal, a second input for receiving the Burst Length attribute signal, a third input for

> receiving the Bus Width signal from an addressed memory, such as memory 22, 24 or 26. A first output of the Dynamic Buffer Configuration logic 72 is connected to an input of Adaptive Buffer Store Replacement logic 74. An output of the Adaptive Buffer Store Replacement logic 74 provides a buffer portion replacement indicator and is connected to a first input of Request Type logic 76. A second output of the Dynamic Buffer Configuration logic 72 is connected to a second input of the Request Type logic 76. An output of the Request Type logic 76 is connected to one of the three Memory Interconnects of FIG. 2.

(*Malik* at paragraphs 16 and 19). *Malik* does not mention registers, much less "registers ... configured to enable the memory device interface to buffer in a ... portion of the buffer data" as alleged. Thus, *Malik* does not disclose or suggest "A memory device interface comprising... a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first data transfer link; and a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link" as recited in claim 15.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 15. Therefore, Applicants respectfully submit that the rejection of claim 15 be withdrawn.

M. Dependent Claims 16-18

Since independent claim 15 is allowable, Applicants respectfully submit that claims 16-18 are allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir.1988). Therefore, Applicants respectfully request that the rejection of claims 16-18 be withdrawn.

N. Dependent Claim 17

Applicants' claim 17 provides as follows (emphasis added):

> ***The memory device interface of claim 15, wherein the first data transfer link is coupled to a first input/output (I/O) device, and the second data transfer link is coupled to a second I/O device.***

Notwithstanding, and in addition to, the arguments discussed above, Applicants respectfully request that the rejection of claim 3 be withdrawn for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in claim 3.

The Office Action alleges that *Malik* teaches all of the features of claim 17 in the "abstract and paragraphs 13-16, 19 and figures 1, 2 and 5" (Office Action at page 11). Specifically, the Office Action alleges that a first I/O device corresponds to element 12 (master 1) of FIG. 1, a memory device interface corresponds to element 20 (memory controller) of FIG. 1, and a second I/O device corresponds to element 14 (master 2) of FIG. 1 (Office Action at pages 2-3).

In particular, *Malik* teaches that:

> any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...
>
> If the address does not hit in the prefetch buffer 30 and misses... prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

(*Malik* at paragraphs 14-15). While *Malik* teaches <u>providing data to</u> the requesting master, *Malik* does not teach or suggest "data received via a ... data transfer link", as recited in parent claim 15, wherein "the data transfer link is coupled to a ... input/output (I/O) device" as recited in claim 17. Under the Examiner's analysis, each limitation of Applicants' claim is being considered independent of the other limitations. Such an approach is improper given that it treats Applicants' claims in a piecemeal fashion such that each limitation is evaluated in a vacuum. As is well established in the law, the Examiner must instead consider the claims as a whole. *Hartness International, Inc. v. Simplimatic Engineering Co.*, 819 F.2d 1100, 2 USPQ2d 1826 (Fed. Cir. 1987) (In determining obviousness, "the inquiry is not whether each element existed in the prior art, but

whether the prior art made obvious the invention as a whole for which patentability is claimed"). When Applicants' claims are considered as a whole, it becomes clear that *Malik* does not teach what the Examiner alleges. Thus, *Malik* does not disclose, teach or suggest the "memory device interface of claim 15, wherein the first data transfer link is coupled to a first input/output (I/O) device, and the second data transfer link is coupled to a second I/O device" as recited in claim 17.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in claim 17. Therefore, Applicants respectfully submit that the rejection of claim 17 be withdrawn.

O. Independent Claim 19

Applicants' amended claim 19 provides as follows (emphasis added):

> A system comprising:
> means for determining at least one characteristic of a first input/output (I/O) device and at least one characteristic of a second I/O device, the first and second I/O devices coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O devices and a memory device;
> ***means for providing buffer allocation information to the first I/O device responsive to the at least one characteristic of the first I/O device and to the second I/O device responsive to the at least one characteristic of the second I/O device***;
> means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion corresponding to the buffer allocation information provided to the first I/O device; and
> means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion corresponding to the second buffer allocation information provided to the second I/O device.

Applicants respectfully submit that amended independent claim 19 is allowable for at least the reason that *Malik* fails to disclose, teach, or suggest at least the features recited and emphasized above in amended claim 19.

While *Malik* discloses:

> In operation, any one of the masters 12, 14 and 16 issues or generates at least one or more data requests to any of the memories 22, 24 and 26 that are addressed by a read request of the memories. ... The read request from the master is seen by the memory controller 20. The read request has one or more attributes such as the Data Size and Burst Length. The memory controller is aware of the master ID, the data size being requested and a requested burst length as well as a memory address. The Burst Length signal communicates to the memory controller 20 whether the requested operation is a burst operation. Based on the information in the memory controller interconnect, if the address hits in the prefetch buffer 30 meaning that the requested data is in the prefetch buffer, the data is provided directly to the switch circuitry 19 and back to the requesting master. ...
>
> If the address does not hit in the prefetch buffer 30 and misses, based on whether the requesting master is enabled for prefetching, dynamic configuration of the prefetch buffer line size occurs based on data size and burst length. An adaptive buffer line replacement algorithm... selects which buffer line is replaced and new data written to. The prefetch control circuitry 32 determines the number and size of the accesses to the memories 22, 24 and 26 based on buffer configuration and memory bus width. The data that is requested is then provided to the requesting master.

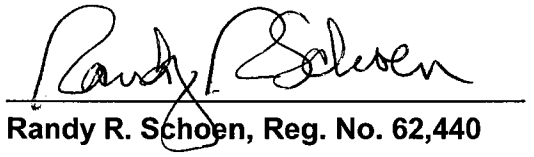
(*Malik* at paragraphs 14-15), *Malik* does not teach or suggest "providing buffer allocation information to the ... I/O device" as recited in amended claim 19. Thus, *Malik* does not disclose, teach or suggest "means for providing buffer allocation information to the first I/O device responsive to the at least one characteristic of the first I/O device and to the second I/O device responsive to the at least one characteristic of the second I/O device" as recited in amended claim 19.

For at least the reasons described above, *Malik* fails to disclose, teach or suggest all of the features recited in amended claim 19. Therefore, Applicants respectfully submit that the rejection of claim 19 be withdrawn.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and presently pending claims 1, 3-6, and 8-19 be allowed to issue. Any statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

By: 

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